Touch Screen Digitizer

AD7873

FEATURES

4-Wire Touch Screen Interface
On-Chip Temperature Sensor: –40°C to +85°C
On-Chip 2.5 V Reference
Direct Battery Measurement (0 V to 6 V)
Touch-Pressure Measurement
Specified Throughput Rate of 125 kSPS
Single Supply, V_{CC} of 2.2 V to 5.25 V
Ratiometric Conversion
High-Speed Serial Interface
Programmable 8- or 12-Bit Resolution
One Auxiliary Analog Input
Shutdown Mode: 1 μA Max
16-Lead QSOP, TSSOP, and LFCSP Packages

APPLICATIONS

Personal Digital Assistants
Smart Hand-Held Devices
Touch Screen Monitors
Point-of-Sale Terminals
Pagers

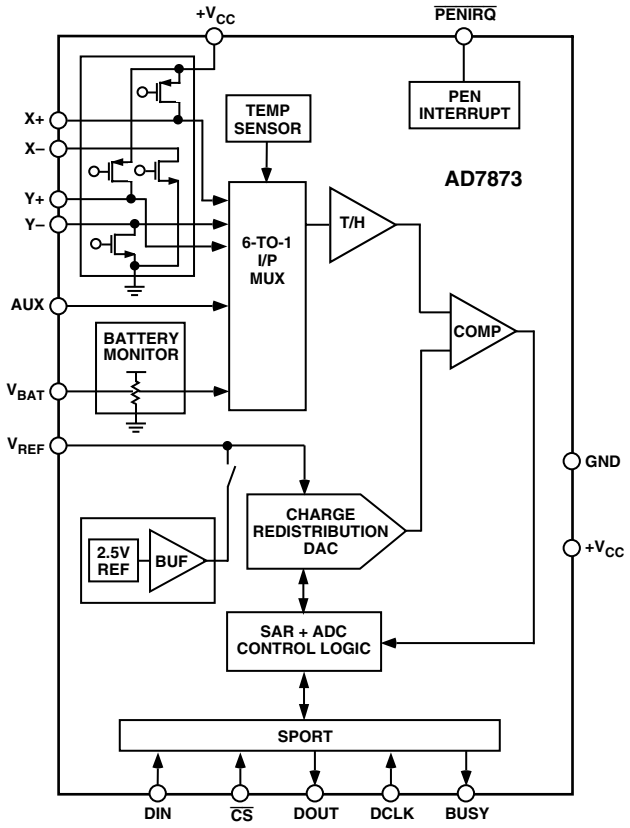
GENERAL DESCRIPTION

The AD7873 is a 12-bit successive-approximation ADC with a synchronous serial interface and low on resistance switches for driving touch screens. The AD7873 operates from a single 2.2 V to 5.25 V power supply and features throughput rates greater than 125 kSPS.

The AD7873 features direct battery measurement, temperature measurement, and touch-pressure measurement. The AD7873 also has an on-board reference of 2.5 V which can be used for the auxiliary input, battery monitor, and temperature measurement modes. When not in use, the internal reference can be shut down to conserve power. An external reference can also be applied and can be varied from 1 V to V_{CC}, while the analog input range is from 0 V to V_{REF}. The device includes a shutdown mode that reduces the current consumption to less than 1 μA.

The AD7873 features on-board switches. This, coupled with low power and high-speed operation, makes the device ideal for battery-powered systems such as personal digital assistants with resistive touch screens and other portable equipment. The part is available in a 16-lead 0.15" Quarter Size Outline (QSOP) package, a 16-lead Thin Shrink Small Outline (TSSOP) package, and a 16-lead Lead Frame Chip Scale (LFCSP) package.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Ratiometric conversion mode available, eliminating errors due to on-board switch resistances
2. On-board temperature sensor: –40°C to +85°C
3. Battery monitor input
4. Touch-pressure measurement capability
5. Low power consumption of 1.37 mW max with the reference off, or 2.41 mW typ with the reference on, at 125 kSPS and V_{CC} at 3.6 V.
6. Package options include 4 mm × 4 mm LFCSP.
7. Analog input range from 0 V to V_{REF}
8. Versatile serial I/O port

REV. B

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AD7873—SPECIFICATIONS

($+V_{CC}$ = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal or external, f_{DCLK} = 2 MHz; T_A = –40°C to +85°C, unless otherwise noted.)

Parameter	AD7873A[1]	AD7873B[1]	Unit	Test Conditions/Comments
DC ACCURACY				
Resolution	12	12	Bits	
No Missing Codes	11	12	Bits min	
Integral Nonlinearity[2]	±2	±1	LSB max	
Differential Nonlinearity[2]		–0.9/+1.5	LSB max	
Offset Error[2]	±6	±6	LSB max	$+V_{CC}$ = 2.7 V
Gain Error[2]	±4	±4	LSB max	External Reference
Noise	70	70	µV rms typ	
Power Supply Rejection	70	70	dB typ	
SWITCH DRIVERS				
On Resistance[2]				
Y+, X+	5	5	Ω typ	
Y–, X–	6	6	Ω typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	
DC Leakage Current	±0.1	±0.1	µA typ	
Input Capacitance	37	37	pF typ	
REFERENCE INPUT/OUTPUT				
Internal Reference Voltage	2.45/2.55	2.45/2.55	V min/max	
Internal Reference Tempco	±15	±15	ppm/°C typ	
V_{REF} Input Voltage Range	$1/V_{CC}$	$1/V_{CC}$	V min/max	
DC Leakage Current	±1	±1	µA max	
V_{REF} Input Impedance	1	1	GΩ typ	$\overline{CS}$ = GND or $+V_{CC}$; Typically 260 Ω when On-Board Reference Enabled
TEMPERATURE MEASUREMENT				
Temperature Range	–40/+85	–40/+85	°C min/max	
Resolution				
Differential Method[3]	1.6	1.6	°C typ	
Single Conversion Method[4]	0.3	0.3	°C typ	
Accuracy				
Differential Method[3]	±2	±2	°C typ	
Single Conversion Method[4]	±2	±2	°C typ	
BATTERY MONITOR				
Input Voltage Range	0/6	0/6	V min/max	
Input Impedance	10	10	kΩ typ	Sampling; 1 GΩ when Battery Monitor OFF
Accuracy	±2.5	±2	% max	External Reference
	±3	±3	% max	Internal Reference
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or $+V_{CC}$
Input Capacitance, C_{IN}[5]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{CC} – 0.2	V_{CC} – 0.2	V min	I_{SOURCE} = 250 µA; V_{CC} = 2.2 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 250 µA
$\overline{PENIRQ}$ Output Low Voltage, V_{OL}	0.4	0.4	V max	100 kΩ Pull-Up; I_{SINK} = 250 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[5]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	12	12	DCLK Cycles max	
Track/Hold Acquisition Time	3	3	DCLK Cycles min	
Throughput Rate	125	125	kSPS max	

Parameter	AD7873A[1]	AD7873B[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS				
$+V_{CC}$ (Specified Performance)	2.7/3.6	2.7/3.6	V min/max	Functional from 2.2 V to 5.25 V
I_{CC}[6]				Digital I/Ps = 0 V or V_{CC}
Normal Mode (f_{SAMPLE} = 125 kSPS)	380	380	μA max	Internal Reference OFF. V_{CC} = 3.6 V, 240 μA typ
	670	670	μA typ	Internal Reference ON. V_{CC} = 3.6 V
Normal Mode (f_{SAMPLE} = 12.5 kSPS)	170	170	μA typ	Internal Reference OFF. V_{CC} = 2.7 V, f_{DCLK} = 200 kHz
Normal Mode (Static)	150	150	μA typ	Internal Reference OFF. V_{CC} = 3.6 V
	580	580	μA typ	Internal Reference ON. V_{CC} = 3.6 V
Shutdown Mode (Static)	1	1	μA max	200 nA typ
Power Dissipation[6]				
Normal Mode (f_{SAMPLE} = 125 kSPS)	1.368	1.368	mW max	V_{CC} = 3.6 V. Internal Reference Disabled
	2.412	2.412	mW typ	V_{CC} = 3.6 V. Internal Reference Enabled
Shutdown	3.6	3.6	μW max	V_{CC} = 3.6 V

NOTES
[1]Temperature range as follows: A, B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Difference between Temp0 and Temp1 measurement. No calibration necessary.
[4]Temperature Drift is –2.1 mV/°C.
[5]Sample tested @ 25°C to ensure compliance.
[6]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] ($T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted; V_{CC} = 2.7 V to 5.25 V, V_{REF} = 2.5 V.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{DCLK}[2]	10	kHz min	
	2	MHz max	
t_{ACQ}	1.5	μs min	Acquisition Time
t_1	10	ns min	$\overline{CS}$ Falling Edge to First DCLK Rising Edge
t_2	60	ns max	$\overline{CS}$ Falling Edge to BUSY Three-State Disabled
t_3[3]	60	ns max	$\overline{CS}$ Falling Edge to DOUT Three-State Disabled
t_4	200	ns min	DCLK High Pulsewidth
t_5	200	ns min	DCLK Low Pulsewidth
t_6	60	ns max	DCLK Falling Edge to BUSY Rising Edge
t_7	10	ns min	Data Setup Time Prior to DCLK Rising Edge
t_8	10	ns min	Data Valid to DCLK Hold Time
t_9[3]	200	ns max	Data Access Time after DCLK Falling Edge
t_{10}	0	ns min	$\overline{CS}$ Rising Edge to DCLK Ignored
t_{11}	100	ns max	$\overline{CS}$ Rising Edge to BUSY High Impedance
t_{12}[4]	100	ns max	$\overline{CS}$ Rising Edge to DOUT High Impedance

NOTES
[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V.
[2]Mark/Space ratio for the DCLK input is 40/60 to 60/40.
[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.4 V or 2.0 V.
[4]t_{12} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{12}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

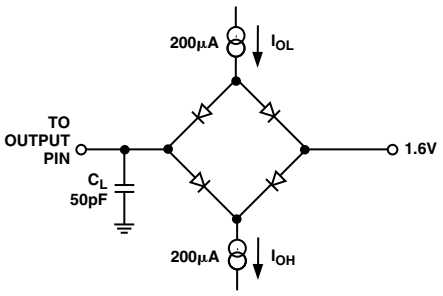
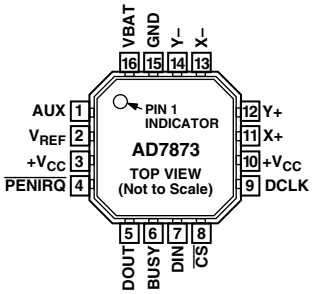


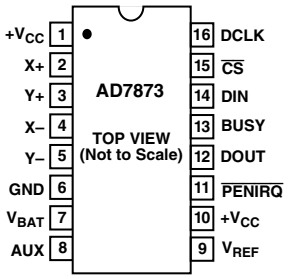
Figure 1. Load Circuit for Digital Output Timing Specifications

PIN CONFIGURATIONS

LFCSP



QSOP, TSSOP



ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted.)

$+V_{CC}$ to GND ..... –0.3 V to +7 V
Analog Input Voltage to GND ..... –0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to GND ..... –0.3 V to V_{CC} + 0.3 V
Digital Output Voltage to GND ..... –0.3 V to V_{CC} + 0.3 V
V_{REF} to GND ..... –0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range
  Commercial (A, B Version) ..... –40°C to +85°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
QSOP, TSSOP, LFCSP Package, Power Dissipation . . 450 mW
  θ_{JA} Thermal Impedance ..... 149.97°C/W (QSOP)
  ..... 150.4°C/W (TSSOP)
  ..... 135.7°C/W (LFCSP)
  θ_{JC} Thermal Impedance ..... 38.8°C/W (QSOP)
  ..... 27.6°C/W (TSSOP)
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latchup.

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[2]	Branding Information
AD7873ARQ	–40°C to +85°C	±2	RQ-16	AD7873ARQ
AD7873ARQ-REEL	–40°C to +85°C	±2	RQ-16	AD7873ARQ
AD7873ARQ-REEL7	–40°C to +85°C	±2	RQ-16	AD7873ARQ
AD7873ARU	–40°C to +85°C	±2	RU-16	AD7873ARU
AD7873ARU-REEL	–40°C to +85°C	±2	RU-16	AD7873ARU
AD7873ARU-REEL7	–40°C to +85°C	±2	RU-16	AD7873ARU
AD7873BRQ	–40°C to +85°C	±1	RQ-16	AD7873BRQ
AD7873BRQ-REEL	–40°C to +85°C	±1	RQ-16	AD7873BRQ
AD7873BRQ-REEL7	–40°C to +85°C	±1	RQ-16	AD7873BRQ
AD7873ACP[5]	–40°C to +85°C	±2	CP-16	AD7873ACP
AD7873ACP-REEL[5]	–40°C to +85°C	±2	CP-16	AD7873ACP
AD7873ACP-REEL7[5]	–40°C to +85°C	±2	CP-16	AD7873ACP
AD7873BCP[5]	–40°C to +85°C	±1	CP-16	AD7873BCP
AD7873BCP-REEL[5]	–40°C to +85°C	±1	CP-16	AD7873BCP
AD7873BCP-REEL7[5]	–40°C to +85°C	±1	CP-16	AD7873BCP
EVAL-AD7873CB[3]	Evaluation Board			
EVAL-CONTROL BRD2[4]	Controller Board			

NOTES
[1]Linearity error here refers to integral linearity error.
[2]RQ = QSOP = 0.15" Quarter Size Outline Package; RU = TSSOP.
[3]This can be used as a standalone evaluation board or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes.
[4]This Evaluation Board Controller is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.
[5]Contact factory for availability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7873 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 10	$+V_{CC}$	Power Supply Input. The $+V_{CC}$ range for the AD7873 is from 2.2 V to 5.25 V. Both $+V_{CC}$ pins should be connected directly together.
2	X+	X+ Position Input. ADC Input Channel 1.
3	Y+	Y+ Position Input. ADC Input Channel 2.
4	X–	X– Position Input
5	Y–	Y– Position Input. ADC Input Channel 3.
6	GND	Analog Ground. Ground reference point for all circuitry on the AD7873. All analog input signals and any external reference signals should be referred to this GND voltage.
7	V_{BAT}	Battery Monitor Input. ADC Input Channel 4.
8	AUX	Auxiliary Input. ADC Input Channel 5.
9	V_{REF}	Reference output for the AD7873. Alternatively an external reference can be applied to this input. The voltage range for the external reference is 1.0 V to $+V_{CC}$. For specified performance it is 2.5 V on the AD7873. The internal 2.5 V reference is available on this pin for use external to the device. The reference output must be buffered before it is applied elsewhere in a system. A capacitor of 0.1 μF is recommended between this pin and GND to reduce system noise effects.
11	$\overline{\text{PENIRQ}}$	Pen Interrupt. CMOS Logic open drain output (requires 10 kΩ to 100 kΩ pull-up resistor externally).
12	DOUT	Data Out. Logic Output. The conversion result from the AD7873 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the DCLK input. This output is high impedance when $\overline{\text{CS}}$ is high.
13	BUSY	BUSY Output. Logic output. This output is high impedance when $\overline{\text{CS}}$ is high.
14	DIN	Data In. Logic Input. Data to be written to the AD7873's control register is provided on this input and is clocked into the register on the rising edge of DCLK (see Control Register section).
15	$\overline{\text{CS}}$	Chip Select Input. Active Low Logic Input. This input provides the dual function of initiating conversions on the AD7873 and also enables the serial input/output register.
16	DCLK	External Clock Input. Logic Input. DCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7873's conversion process.

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Gain Error

This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

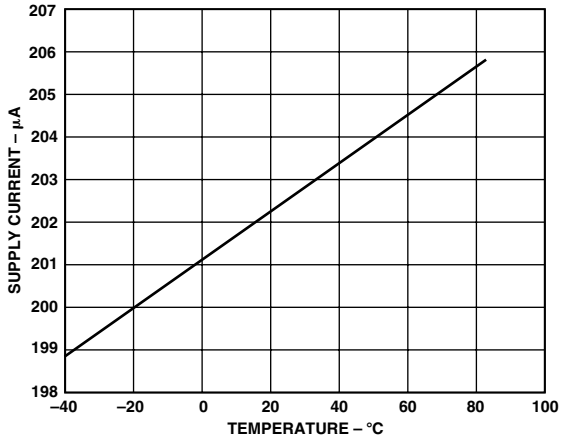
Track/Hold Acquisition Time

The track/hold amplifier enters the acquisition phase on the fifth falling edge of DCLK after the START bit has been detected. Three DCLK cycles are allowed for the Track/Hold acquisition time and the input signal will be fully acquired to the 12-bit level within this time even with the maximum specified DCLK frequency. See Analog Input section for more details.

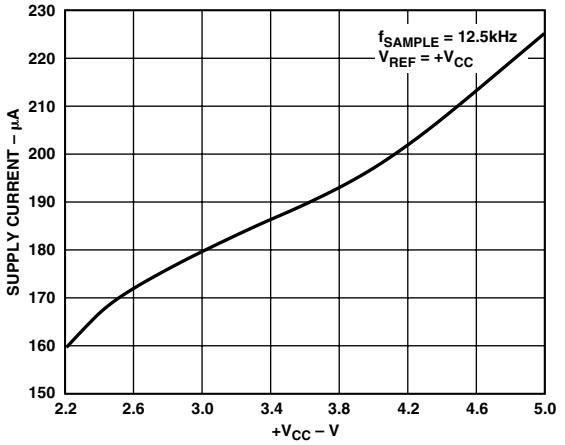
On Resistance

This is a measure of the ohmic resistance between the drain and source of the switch drivers.

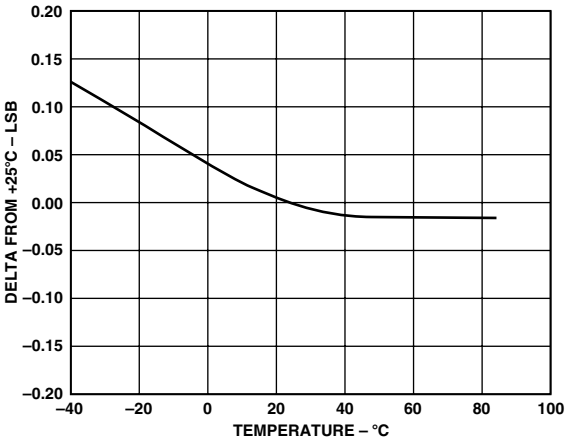
AD7873–Typical Performance Characteristics



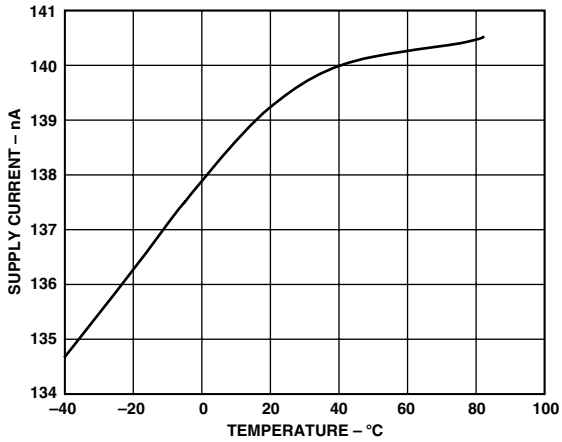
TPC 1. Supply Current vs. Temperature



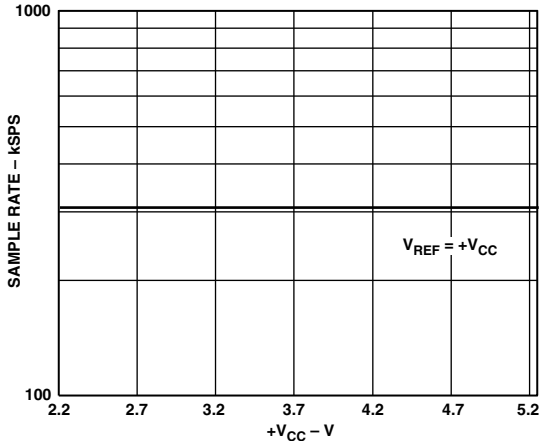
TPC 2. Supply Current vs. $+V_{CC}$



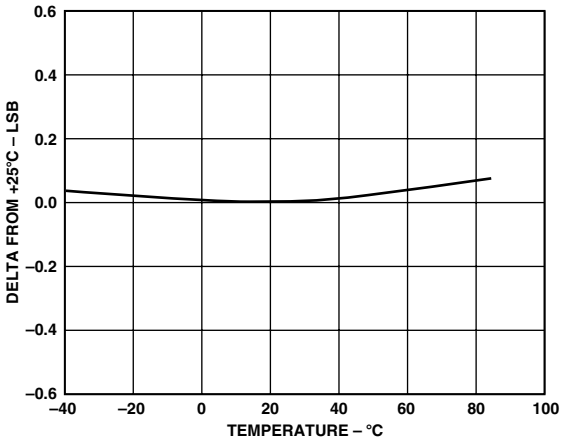
TPC 3. Change in Gain vs. Temperature



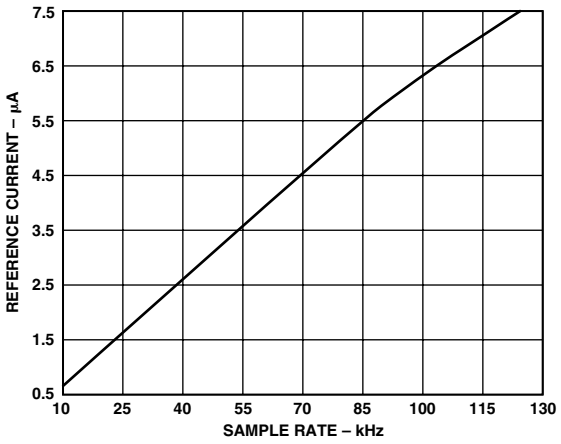
TPC 4. Power-Down Supply Current vs. Temperature



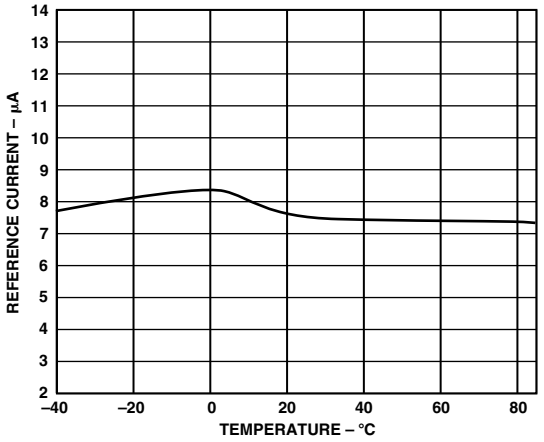
TPC 5. Maximum Sample Rate vs. $+V_{CC}$



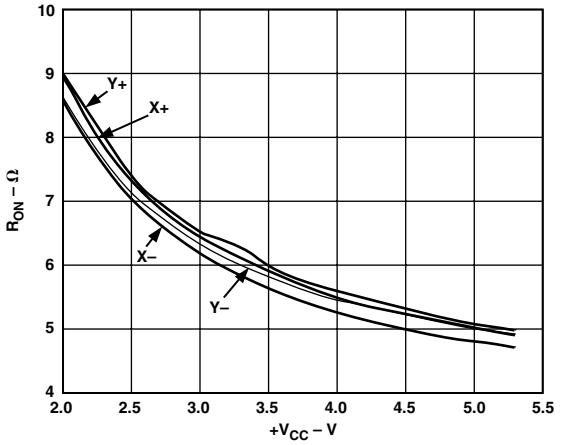
TPC 6. Change in Offset vs. Temperature



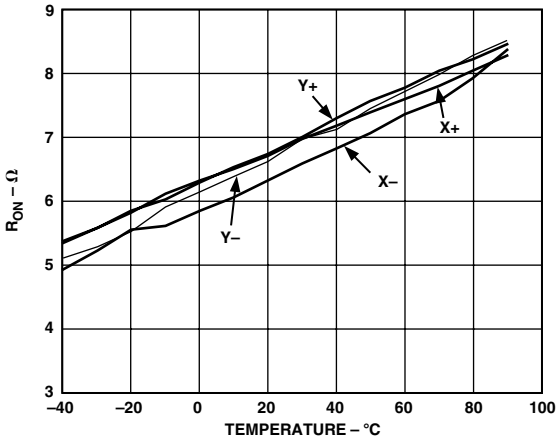
TPC 7. Reference Current vs. Sample Rate



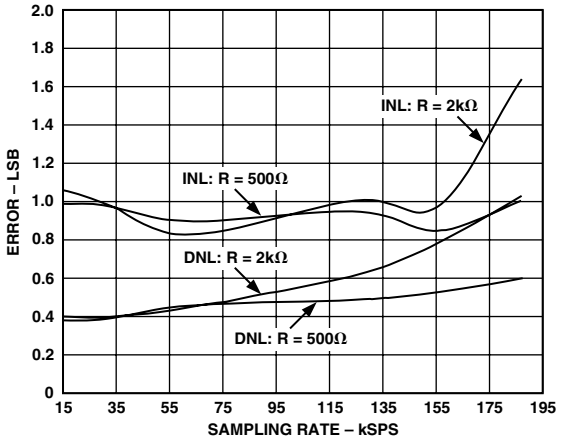
TPC 10. Reference Current vs. Temperature



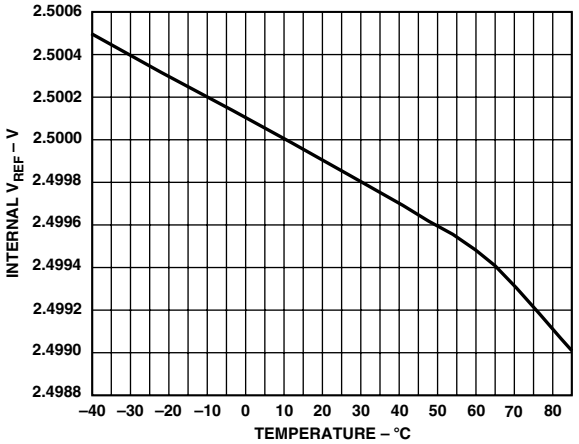
TPC 8. Switch On Resistance vs. $+V_{CC}$ ($X+$, $Y+$: $+V_{CC}$ to Pin; $X–$, $Y–$: Pin to GND)



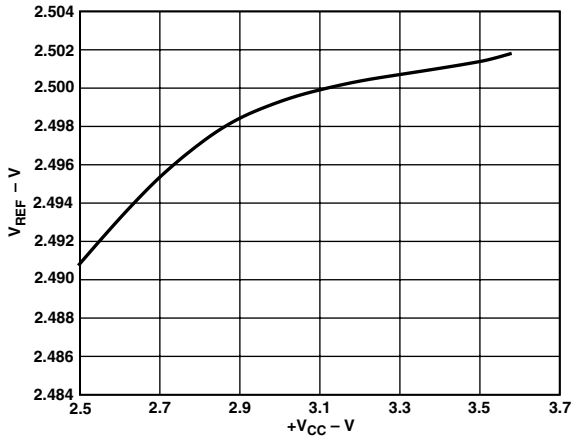
TPC 11. Switch On Resistance vs. Temperature ($X+$, $Y+$: $+V_{CC}$ to Pin; $X–$, $Y–$: Pin to GND)



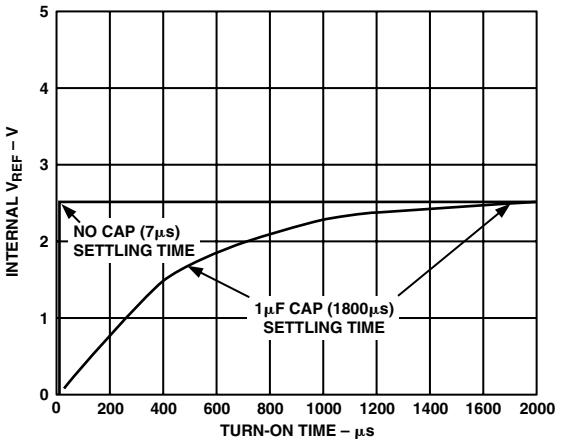
TPC 9. Maximum Sampling Rate vs. R_{IN}



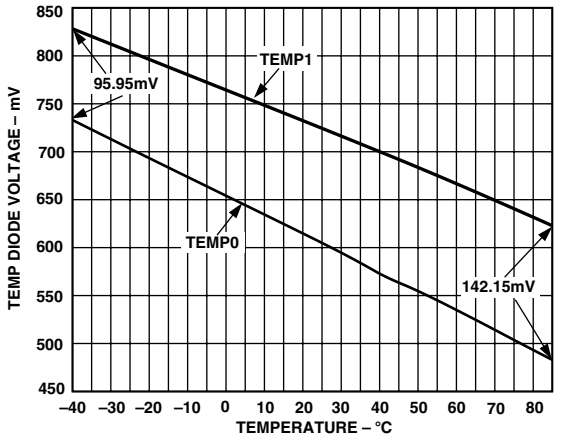
TPC 12. Internal V_{REF} vs. Temperature



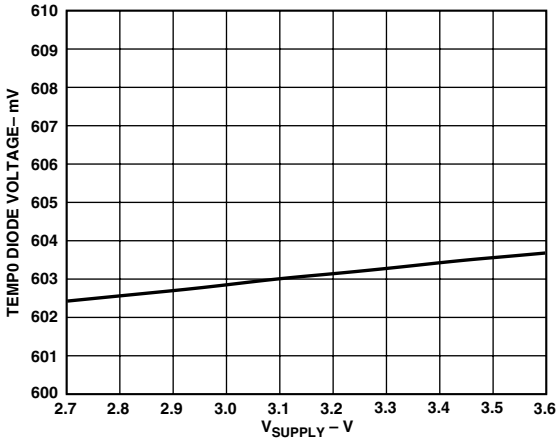
TPC 13. Internal V_{REF} vs. $+V_{CC}$



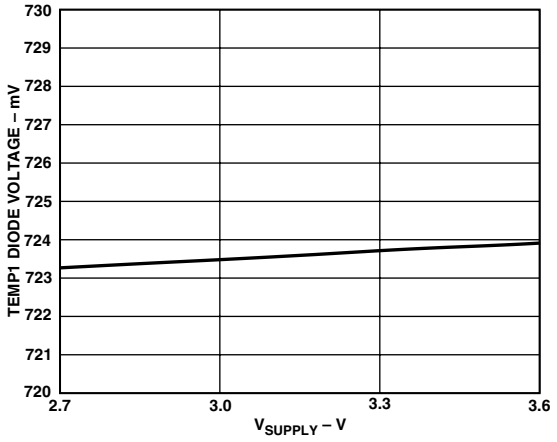
TPC 16. Internal V_{REF} vs. Turn-on Time



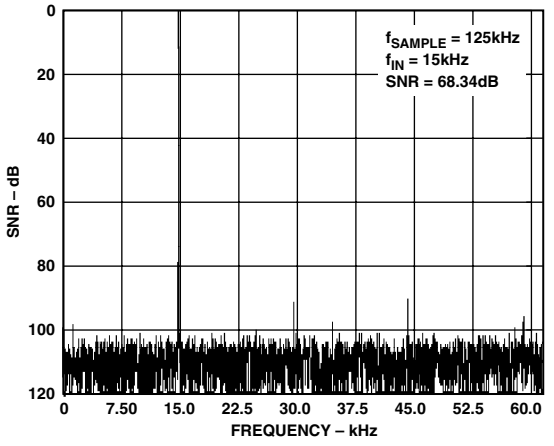
TPC 14. Temp Diode Voltage vs. Temperature (2.7 V Supply)



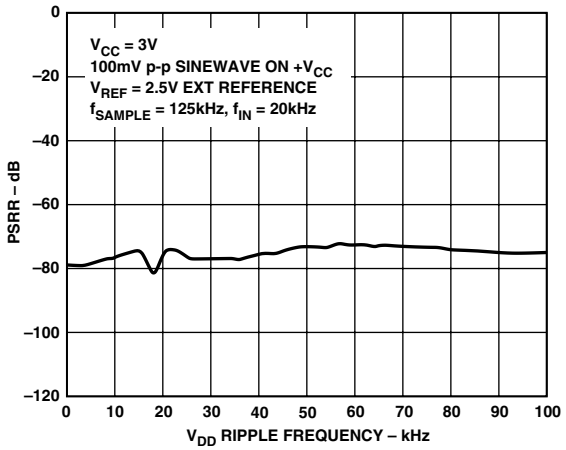
TPC 17. Temp0 Diode Voltage vs. V_{SUPPLY} (25°C)



TPC 15. Temp1 Diode Voltage vs. V_{SUPPLY} (25°C)



TPC 18. Auxiliary Channel Dynamic Performance



TPC 19. AC PSRR vs. Supply Ripple Frequency

TPC 18 shows a typical FFT plot for the auxiliary channels of the AD7873 at 125 kHz sample rate and 15 kHz input frequency.

TPC 19 shows the power supply rejection ratio versus V_{DD} supply frequency for the AD7873. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency f, to the power of a 100 mV sine wave applied to the ADC V_{CC} supply of frequency f_S:

$$PSRR\ (dB) = 10\ log\ (Pf/Pfs)$$

Pf = Power at frequency f in ADC output, *Pfs* = power at frequency f_S coupled onto the ADC V_{CC} supply. Here a 100 mV peak-to-peak sine wave is coupled onto the V_{CC} supply. Decoupling capacitors of 10 µF and 0.1 µF were used on the supply.

CIRCUIT INFORMATION

The AD7873 is a fast, low-power, 12-bit, single-supply A/D converter. The AD7873 can be operated from a 2.2 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7873 is capable of throughput rates of 125 kSPS when provided with a 2 MHz clock.

The AD7873 provides the user with an on-chip track/hold, multiplexer, A/D converter, reference, temperature sensor, and serial interface housed in a tiny 16-lead QSOP, TSSOP, or LFCSP package, which offers the user considerable space-saving advantages over alternative solutions. The serial clock input (DCLK) accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 V to V_{REF} (where the externally applied V_{REF} can be between 1 V and +V_{CC}). The AD7873 has a 2.5 V reference on board with this reference voltage available for use externally if buffered.

The analog input to the ADC is provided via an on-chip multiplexer. This analog input may be any one of the X, Y, and Z panel coordinates, battery voltage, or chip temperature. The multiplexer is configured with low-resistance switches that allow an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. For some measurements the on resistance of the switches may present a source of error. However, with a differential input to the converter and a differential reference architecture this error can be negated.

ADC TRANSFER FUNCTION

The output coding of the AD7873 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is = V_{REF}/4096. The ideal transfer characteristic for the AD7873 is shown in Figure 2.

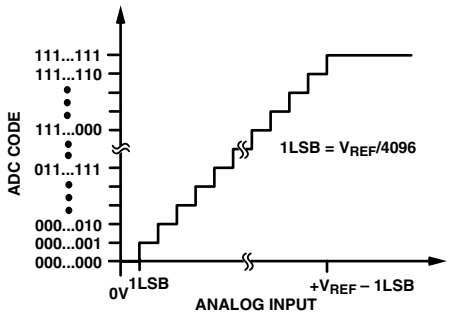


Figure 2. Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 3 shows a typical connection diagram for the AD7873 in a touch screen control application. The AD7873 features an internal reference but this can be overdriven with an external low impedance source between 1 V and +V_{CC}. The value of the reference voltage will set the input range of the converter. The conversion result is output MSB first, followed by the remaining 11 bits and three trailing zeroes, depending on the number of clocks used per conversion (see the Serial Interface section). For applications where power consumption is of concern, the power management option should be used to improve power performance. See Table III for available power management options.

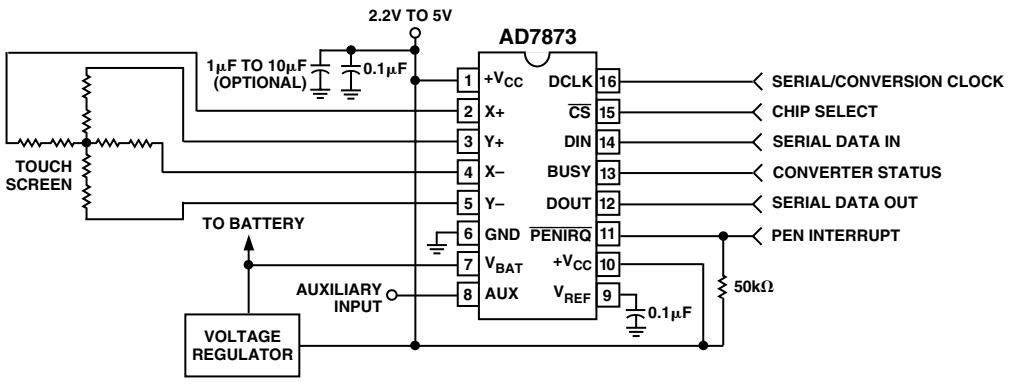


Figure 3. Typical Application Circuit

ANALOG INPUT

Figure 4 shows an equivalent circuit of the analog input structure of the AD7873 that contains a block diagram of the input multiplexer, the differential input of the A/D converter, and the differential reference.

Table I shows the multiplexer address corresponding to each analog input, both for the SER/$\overline{\text{DFR}}$ bit in the control register set high and low. The control bits are provided serially to the device via the DIN pin. For more information on the control register, see the Control Register section.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 4) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 37 pF). Once the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

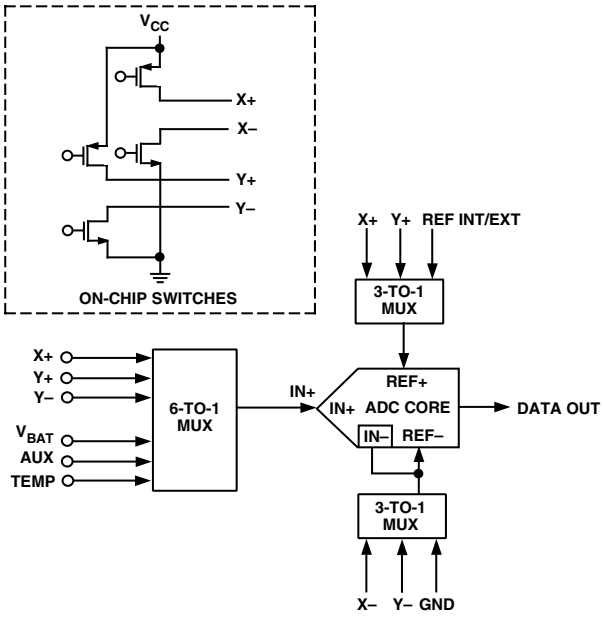


Figure 4. Equivalent Analog Input Circuit

Table I. Analog Input, Reference, and Touch Screen Control

A2	A1	A0	SER/ $\overline{\text{DFR}}$	ANALOG IN	X SWITCHES	Y SWITCHES	+REF*	–REF*
0	0	0	1	TEMP0	OFF	OFF	V_{REF}	GND
0	0	1	1	X+	OFF	ON	V_{REF}	GND
0	1	0	1	VBAT	OFF	OFF	V_{REF}	GND
0	1	1	1	X+ (Z1)	X+ OFF X– ON	Y+ ON Y– OFF	V_{REF}	GND
1	0	0	1	Y– (Z2)	X+ OFF X– ON	Y+ ON Y– OFF	V_{REF}	GND
1	0	1	1	Y+	ON	OFF	V_{REF}	GND
1	1	0	1	AUX	OFF	OFF	V_{REF}	GND
1	1	1	1	TEMP1	OFF	OFF	V_{REF}	GND
0	0	0	0	**Invalid Address. Test Mode: Switches out the Temp0 diode to the $\overline{\text{PENIRQ}}$ pin.**				
0	0	1	0	X+	OFF	ON	Y+	Y–
0	1	0	0	**Invalid Address**				
0	1	1	0	X+ (Z1)	X+ OFF X– ON	Y+ ON Y– OFF	Y+	X–
1	0	0	0	Y– (Z2)	X+ OFF X– ON	Y+ ON Y– OFF	Y+	X–
1	0	1	0	Y+	ON	OFF	X+	X–
1	1	0	0	**Outputs Identity Code, 1000 0000 0000.**				
1	1	1	0	**Invalid address. Test mode: Switches out the Temp1 diode to the $\overline{\text{PENIRQ}}$ pin.**				

*Internal node, not directly accessible by the user.

Acquisition Time

The track-and-hold amplifier enters its tracking mode on the falling edge of the fifth DCLK after the START bit has been detected (see Figure 13). The time required for the track-and-hold amplifier to acquire an input signal will depend on how quickly the 37 pF input capacitance is charged. With zero source impedance on the analog input, three DCLK cycles will always be sufficient to acquire the signal to the 12-bit level. With a source impedance R_{IN} on the analog input, the actual acquisition time required is calculated using the formula:

$$t_{ACQ} = 8.4 \times (R_{IN} + 100\ \Omega) \times 37\ pF$$

where R_{IN} is the source impedance of the input signal, and 100 Ω, 37 pF is the input RC. Depending on the frequency of DCLK used, three DCLK cycles may or may not be sufficient to acquire the analog input signal with various source impedance values.

Touch Screen Settling

In some applications, external capacitors may be required across the touch screen to filter noise associated with it, e.g., noise generated by the LCD panel or backlight circuitry. The value of these capacitors will cause a settling time requirement when the panel is touched. The settling time will typically show up as a gain error. There are several methods for minimizing or eliminating this issue. The problem may be that the input signal, reference, or both, have not settled to their final value before the sampling instant of the ADC. Additionally, the reference voltage may still be changing during the conversion cycle. One option is to stop, or slow down, the DCLK for the required touch screen settling time. This will allow the input and reference to stabilize for the acquisition time. This will resolve the issue for both single-ended and differential modes.

The other option is to operate the AD7873 in differential mode only for the touch screen, and program the AD7873 to keep the touch screen drivers on and not go into power-down (PD0 = PD1 = 1). Several conversions may be required, depending on the settling time required and the AD7873 data rate. Once the required number of conversions have been made, the AD7873 can then be placed in a power-down state on the last measurement. The last method is to use the 15 DCLK cycle mode which maintains the touch screen drivers on until it is commanded by the processor to stop.

Internal Reference

The AD7873 has an internal reference voltage of 2.5 V. The internal reference is available on the V_{REF} pin for external use in the system; however, it must be buffered before it is applied elsewhere. The on-chip reference can be turned ON or OFF with the power-down address, PD1 = 1 (see Table III and Figure 5). Typically the reference voltage is only used in the single-ended mode for battery monitoring, temperature measurement, and for using the auxiliary input. Optimal touch screen performance is achieved when using the differential mode. The power-up time of the 2.5 V reference is typically 10 µs without a load; however, a 0.1 µF capacitor on the V_{REF} pin is recommended for optimum performance, which will affect the power-up time. (See TPC 16.)

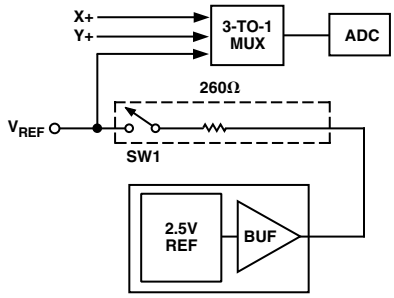


Figure 5. On-Chip Reference Circuitry

Reference Input

The voltage difference between +REF and –REF (see Figure 4) sets the analog input range. The AD7873 will operate with a reference input in the range of 1 V to $+V_{CC}$. Figure 5 shows the on-chip reference circuitry on the AD7873. The internal reference on the AD7873 can be overdriven with an external reference; for best performance, however, the internal reference should be disabled when an external reference is applied, as SW1 in Figure 5 will open on the AD7873 when the internal reference is disabled. The on-chip reference will always be available at the V_{REF} pin as long as the reference is enabled. The input impedance seen at the V_{REF} pin is approximately 260 Ω when the internal reference is enabled. When it is disabled, the input impedance seen at the V_{REF} pin will be in the gigaohm region.

When making touch screen measurements, conversions can be made in the differential (ratiometric) mode or the single-ended mode. If the SER/$\overline{\text{DFR}}$ bit is set to 1 in the control register, then a single-ended conversion will be performed. Figure 6 shows the configuration for a single-ended Y coordinate measurement. The X+ input is connected to the analog-to-digital converter, the Y+ and Y– drivers are turned on, and the voltage on X+ is digitized. The conversion is performed with the ADC referenced from GND to V_{REF}. This V_{REF} will either be the on-chip reference or the voltage applied at the V_{REF} pin externally, and is determined by the setting of the power management bits PD0 and PD1 (see Table II). The advantage of this mode is that the switches that supply the external touch screen can be turned off once the acquisition is complete, resulting in a power savings. However, the on resistance of the Y drivers will affect the input voltage that can be acquired. The full touch screen resistance may be in the order of 200 Ω to 900 Ω, depending on the manufacturer. Thus, if the on resistance of the switches is approximately 6 Ω, then true full-scale and zero-scale voltages cannot be acquired, regardless of where the pen/stylus is on the touch screen. Note, the minimum touch screen resistance recommended for use with the AD7873 is approximately 70 Ω. In this mode of operation, therefore, some voltage is likely to be lost across the internal switches and it is unlikely that the internal switch resistance will track the resistance of the touch screen over temperature and supply, providing an additional source of error.

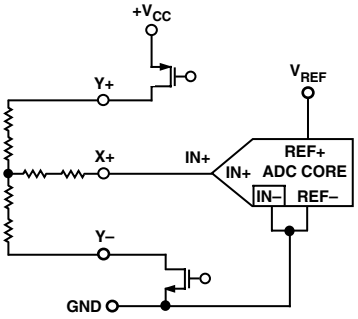


Figure 6. Single-Ended Reference Mode (SER/$\overline{DFR}$ = 1)

The alternative to this situation is to set the SER/$\overline{DFR}$ bit low. Again, making a Y coordinate measurement is considered, but now the +REF and –REF nodes of the ADC are connected directly to the Y+ and Y– pins. This means the analog-to-digital conversion will be ratiometric. The result of the conversion will always be a percentage of the external resistance, independent of how it may change with respect to the on resistance of the internal switches. Figure 7 shows the configuration for a ratiometric Y coordinate measurement.

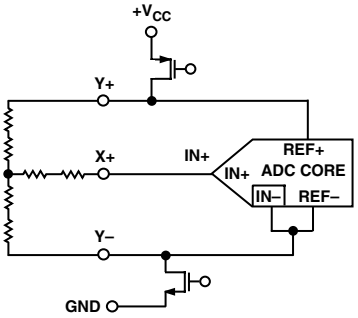


Figure 7. Differential Reference Mode (SER/$\overline{DFR}$ = 0)

The disadvantage of this mode of operation is that during both the acquisition phase and conversion process, the external touch screen must remain powered. This will result in additional supply current for the duration of the conversion.

TEMPERATURE MEASUREMENT

Two temperature measurement options are available on the AD7873, the single conversion method and the differential conversion method. Both methods are based on an on-chip diode measurement.

In the single conversion method, a diode voltage is digitized and recorded at a fixed calibration temperature. Any subsequent polling of the diode will provide an estimate of the ambient temperature through extrapolation from the calibration temperature diode result. This assumes a diode temperature drift of approximately –2.1 mV/°C. This method provides a resolution of approximately 0.3°C and a predicted accuracy of ±3°C.

The differential conversion method is a two-point measurement. The first measurement is performed with a fixed bias current into a diode and the second measurement is performed with a fixed multiple of the bias current into the same diode. The voltage difference in the diode readings is proportional to absolute temperature and is given by the following formula:

$$\Delta V_{BE} = (kT/q) \times (ln\ N)$$

where V_{BE} represents the diode voltage, N is the bias current multiple, k is Boltzmann's constant and q is the electron charge. This method provides more accurate absolute temperature measurement of ±2°C. However, the resolution is reduced to approximately 1.6°C. Assuming a current multiple of 105 (which is typical for the AD7873) taking Boltzmann's constant, $k = 1.38054 \times 10^{-23}$ electrons volts/degrees Kelvin, the electron charge $q = 1.602189 \times 10^{-19}$, then T, the ambient temperature in degrees centigrade, would be calculated as follows:

$$\Delta V_{BE} = (kT/q) \times (ln\ N)$$

$$T = (\Delta V_{BE} \times q)/(k \times ln\ N)$$

$$T°C = 2.49 \times 10^3 \times \Delta V_{BE} - 273K$$

ΔV_{BE} is calculated from the difference in readings from the first conversion and second conversion.

Figure 8 shows a block diagram of the temperature measurement mode.

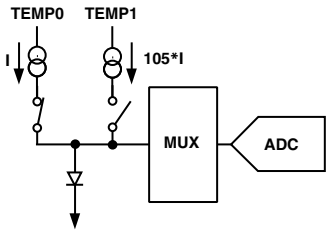


Figure 8. Block Diagram of Temperature Measurement Circuit

BATTERY MEASUREMENT

The AD7873 can monitor a battery voltage from 0 V to 6 V. Figure 9 shows a block diagram of a battery voltage monitored through the V_{BAT} pin. The voltage to the $+V_{CC}$ of the AD7873 is maintained at the desired supply voltage via the dc/dc regulator while the input to the regulator is monitored. This voltage on V_{BAT} is divided by 4 so that a 6 V battery voltage is presented to the ADC as 1.5 V. To conserve power, the divider is only on during the sampling of a voltage on V_{BAT}. Table I shows the control bit settings required to perform a battery measurement.

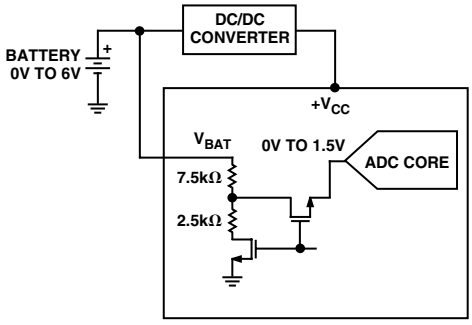


Figure 9. Block Diagram of Battery Measurement Circuit

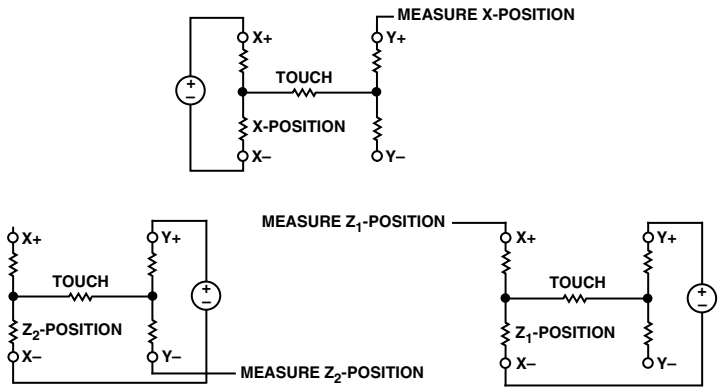


Figure 10. Pressure Measurement Block Diagrams

PRESSURE MEASUREMENT

The pressure applied to the touch screen via a pen or finger may also be measured with the AD7873 with some simple calculations. The 8-bit resolution mode would be sufficient for this measurement, but the following calculations are shown with the 12-bit resolution mode. The contact resistance between the X and Y plates is measured. This provides a good indication of the size of the depressed area and the applied pressure. The area of the spot touched is proportional to the size of the object touching it. The size of this resistance (R_{TOUCH}) can be calculated using two different methods.

The first method requires the user to know the total resistance of the X-plate tablet. Three touch screen conversions are required, a measurement of the X-position, Z_1-position and Z_2-position (see Figure 10). The following equation will calculate the touch resistance:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION}/4095) \times [(Z_2/Z_{1)} - 1]$$

The second method requires that the resistance of both the X-plate and Y-plate tablets are known. Again three touch screen conversions are required, a measurement of the X-position, Y-position, and Z_1-position (see Figure 10).

The following equation will also calculate the touch resistance:

$$R_{TOUCH} = \{(R_{XPLATE}/Z_1) \times (X_{POSITION}/4095) \times [(4096/Z_1) - 1]\} - \{R_{YPLATE} \times (Y_{POSITION}/4095)\}$$

PEN INTERRUPT REQUEST

The pen interrupt equivalent output circuitry is outlined in Figure 11. By connecting a pull-up resistor (10 kΩ to 100 kΩ) between $+V_{CC}$ and this CMOS Logic open drain output, the $\overline{\text{PENIRQ}}$ output will remain high normally. If $\overline{\text{PENIRQ}}$ has been enabled (see Table III), when the touch screen connected to the AD7873 is touched by a pen or finger, the $\overline{\text{PENIRQ}}$ output will go low, initiating an interrupt to a microprocessor that may then instruct a control word to be written to the AD7873 to initiate a conversion. This output can also be enabled between conversions during power-down (see Table III) allowing power-up to be initiated only when the screen is touched. The result of the first touch screen coordinate conversion after power-up will be valid assuming any external reference is settled to the 12- or 8-bit level as required.

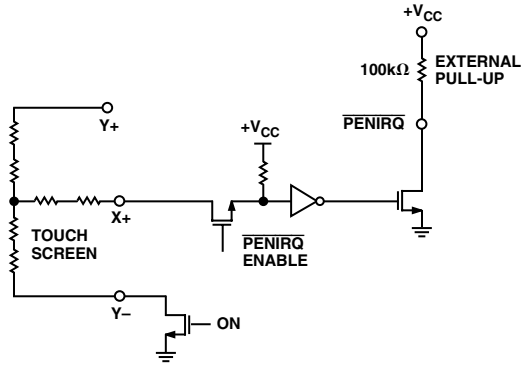


Figure 11. $\overline{\text{PENIRQ}}$ Functional Block Diagram

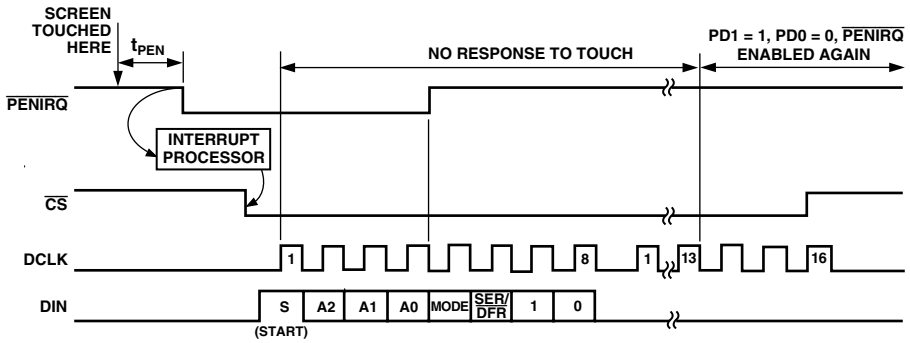


Figure 12. PENIRQ Timing Diagram

Figure 12 assumes the PENIRQ function has been enabled in the last write or the part has just been powered up so PENIRQ is enabled by default. Once the screen is touched, the PENIRQ output will go low a time t_{PEN} later. This delay is approximately 5 µs, assuming a 10 nF touch screen capacitance, and will vary with the touch screen resistance actually used. Once the START bit is detected the pen interrupt function is disabled and the PENIRQ will not respond to screen touches. The PENIRQ output will remain low until the fourth falling edge of DCLK after the START bit has been clocked in, at which point it will return high as soon as possible, irrespective of the touch screen capacitance. This does not mean the pen interrupt function is now enabled again as the power-down bits have not yet been loaded to the control register. So regardless of whether PENIRQ is to be enabled again, the PENIRQ output will always idle high normally. Assuming the PENIRQ is enabled again as shown in Figure 12, then once the conversion is complete, the PENIRQ output will again respond to a screen touch. The fact that PENIRQ returns high almost immediately after the fourth falling edge of DCLK means the user will avoid any spurious interrupts on the microprocessor or DSP that could occur if the interrupt request line on the micro/DSP were unmasked during or toward the end of conversion and the PENIRQ pin was still low. Once the next START bit is detected by the AD7843 the PENIRQ function is again disabled.

If the control register write operation will overlap with the data read, a START bit will always be detected prior to the end of conversion, meaning that even if the PENIRQ function has been enabled in the control register it will be disabled by the START bit again before the end of the conversion is reached, so the PENIRQ function effectively cannot be used in this mode. However, as conversions are occurring continuously, the PENIRQ function is not necessary and is therefore redundant.

CONTROL REGISTER

The control word provided to the ADC via the DIN pin is shown in Table II. This provides the conversion start, channel addressing, ADC conversion resolution, configuration, and power-down of the AD7873. Table II provides detailed information on the order and description of these control bits within the control word.

Initiate START

The first bit, the 'S' bit, must always be set to 1 to initiate the start of the control word. The AD7873 will ignore any inputs on the DIN line until the start bit is detected.

Channel Addressing

The next three bits in the control register, A2, A1, and A0, select the active input channel(s) of the input multiplexer (see Table I and Figure 4), touch screen drivers, and the reference inputs.

MODE

The MODE bit sets the resolution of the analog-to-digital converter. With a 0 in this bit, the following conversion will have 12 bits of resolution. With a 1 in this bit, the following conversion will have 8 bits of resolution.

SER/DFR

The SER/DFR bit controls the reference mode, which can be either single-ended or differential if a 1 or a 0 is written to this bit respectively. The differential mode is also referred to as the ratiometric conversion mode. This mode is optimum for X-position, Y-position, and pressure-touch measurements. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a separate reference voltage is not needed as the reference voltage to the analog-to-digital converter is the voltage across the touch screen. In the single-ended mode, the reference voltage to the converter is always the difference between the V_{REF} and GND pins. See Table I and Figures 4 through 7 for further information.

If X-position, Y-position, and pressure touch are measured in the single-ended mode, an external reference voltage or $+V_{CC}$ is required for maximum dynamic range. The internal reference can be used for these single-ended measurements, however a loss in dynamic range will be incurred. If an external reference is used, the AD7873 should also be powered from the external reference. As the supply current required by the device is so low, a precision reference can be used as the supply source to the AD7873. It may also be necessary to power the touch screen from the reference which may require 5 mA to 10 mA. A REF19x voltage reference can source up to 30 mA and as such could supply both the ADC and the touch screen. Care must be taken however, to ensure that the input voltage applied to the ADC does not exceed the reference voltage and hence the supply voltage. See Absolute Maximum Ratings section.

NOTE: The differential mode can only be used for X-position, Y-position, and pressure touch measurements. All other measurements require the single-ended mode.

PD0 and PD1

The power management options are selected by programming the power management bits, PD0 and PD1, in the control register. Table III summarizes the options available and the internal reference voltage configurations. The internal reference can be turned ON or OFF independent of the analog-to-digital converter, allowing power saving between conversions using the power management options.

Table II. Control Register Bit Function Description

MSB							LSB
S	A2	A1	A0	MODE	SER/DFR	PD1	PD0

Bit	Mnemonic	Comment
7	S	Start Bit. The control word starts with the first high bit on DIN. A new control word can start every fifteenth DCLK cycle when in the 12-bit conversion mode or every eleventh DCLK cycle when in 8-bit conversion mode.
6–4	A2–A0	Channel Select Bits. These three address bits along with the SER/$\overline{\text{DFR}}$ bit control the setting of the multiplexer input, switches, and reference inputs, as detailed in Table I.
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the resolution of the following conversion. With a 0 in this bit, the conversion will have 12-bit resolution or, with a 1 in this bit, 8-bit resolution.
2	SER/$\overline{\text{DFR}}$	Single-Ended/Differential Reference Select Bit. Along with bits A2–A0, this bit controls the setting of the multiplexer input, switches, and reference inputs as described in Table I.
1, 0	PD1, PD0	Power Management Bits. These two bits decode the power-down mode of the AD7873 as shown in Table III.

Table III. Power Management Options

PD1	PD0	$\overline{\text{PENIRQ}}$	Description
0	0	Enabled	This configuration will result in immediate power-down of the on-chip reference as soon as PD1 is set to 0. The ADC will only power down between conversions. When PD0 is set to 0 the conversion will be performed first and the ADC will power down upon completion of that conversion (or upon the rising edge of $\overline{\text{CS}}$ if it occurs first). At the start of the next conversion, the ADC instantly powers up to full power. This means if the device is being used in the differential mode, or an external reference is used, there is no need for additional delays to ensure full operation and the very first conversion is valid. The Y– switch is ON while in power-down. When the device is performing differential table conversions, the reference and reference buffer will not attempt to power up with bits PD1 and PD0 programmed in this way.
0	1	Enabled	This configuration will result in switching the reference OFF immediately and the ADC ON permanently. When the device is performing differential tablet conversions, the reference and reference buffer will not attempt to power up with bits PD1 and PD0 programmed in this way.
1	0	Enabled	This configuration will result in switching the reference ON and powering the ADC down between conversions. The ADC will only power down between conversions. When PD0 is set to 0 the conversion will be performed first and the ADC will power down upon completion of that conversion (or upon the rising edge of CS if it occurs first). At the start of the next conversion, the ADC instantly powers up to full power. There is no need for additional delays to ensure full operation as the reference remains permanently powered up.
1	1	Disabled	This configuration will result in keeping the device always powered up. The reference and the ADC are ON.

POWER vs. THROUGHPUT RATE

By using the power-down options on the AD7873 when not converting, the average power consumption of the device decreases at lower throughput rates. Figure 13 shows how, as the throughput rate is reduced, while maintaining the DCLK frequency at 2 MHz, the device remains in its power-down state longer and the average current consumption over time drops accordingly.

For example, if the AD7873 is operated in a 24 DCLK continuous sampling mode, with a throughput rate of 10 kSPS and a DCLK of 2 MHz, and the device is placed in the power-down mode between conversions, (PD0, PD1 = 0, 0), i.e., the ADC will shut down between conversions but the reference will remain powered down permanently, then the current consumption is calculated as follows. The current consumption during normal operation with a 2 MHz DCLK is 210 μA (V_{CC} = 2.7 V). Assuming an external reference is used, the power-up time of the ADC is instantaneous, so when the part is converting it will consume 210 μA. In this mode of operation the part powers up on the fourth falling edge of DCLK after the start bit has been recognized. It goes back into power-down at the end of conversion on the twentieth falling edge of DCLK. This means the part will consume 210 μA for 16 DCLK cycles only, 8 μs, during each conversion cycle. If the throughput rate is 10 kSPS, the cycle time is 100 μs and the average power dissipated during each cycle is (8/100) × (210 μA) = 16.8 μA.

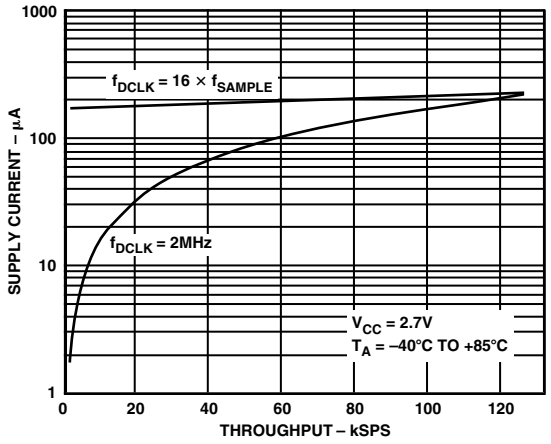


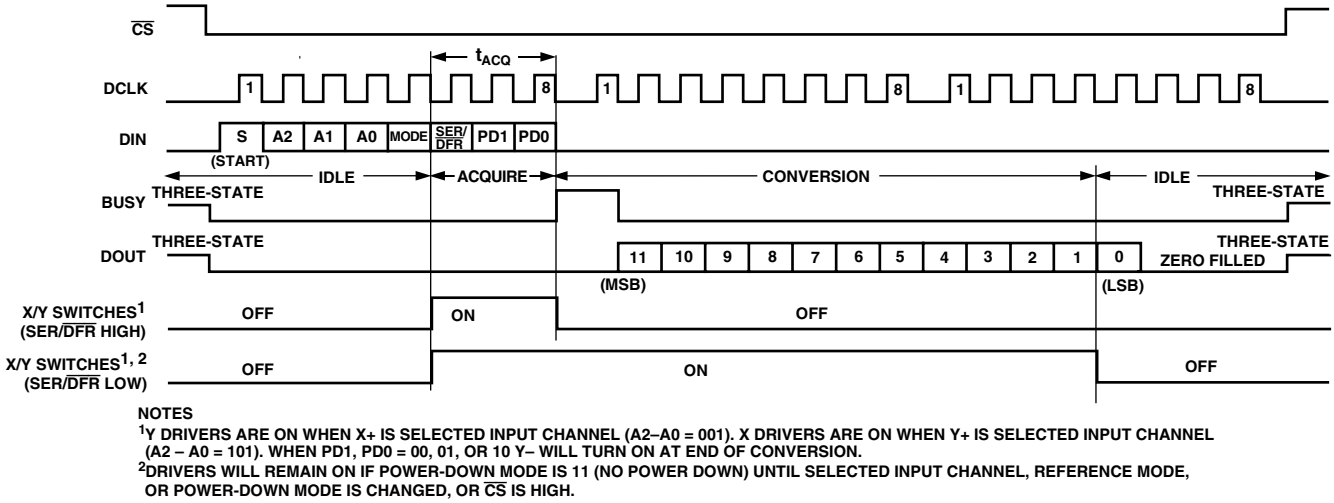
Figure 13. Supply Current vs. Throughput (μA)

SERIAL INTERFACE

Figure 14 shows the typical operation of the serial interface of the AD7873. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7873. One complete conversion can be achieved with 24 DCLK cycles.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ takes the BUSY output and the serial bus out of three-state. The first eight DCLK cycles are used to write to the control register via the DIN pin. The control register is updated in stages as each bit is clocked in and once the converter has enough information about the following conversion to set the input multiplexer and switches appropriately, the converter enters the acquisition mode and if required, the internal switches are turned on. During the acquisition mode the reference input data is updated. After the three DCLK cycles of acquisition, the control word is complete (the power management bits are now updated) and the converter enters the conversion mode. At this point the track and hold goes into hold mode and the input signal is sampled and the BUSY output goes high (BUSY will return low on the next falling edge of DCLK). The internal switches may also turn off at this point if in single-ended mode, battery-monitor mode, or temperature measurement mode.

The next 12 DCLK cycles are used to perform the conversion and to clock out the conversion result. If the conversion is ratiometric (SER/$\overline{DFR}$ LOW), the internal switches are on during the conversion. A thirteenth DCLK cycle is needed to allow the DSP/micro to clock the LSB in. Three more DCLK cycles will clock out the three trailing zeroes and complete the 24 DCLK transfer. The 24 DCLK cycles may be provided from a DSP or via three bursts of eight clock cycles from a microcontroller.



NOTES

[1]Y DRIVERS ARE ON WHEN X+ IS SELECTED INPUT CHANNEL (A2–A0 = 001). X DRIVERS ARE ON WHEN Y+ IS SELECTED INPUT CHANNEL (A2 – A0 = 101). WHEN PD1, PD0 = 00, 01, OR 10 Y– WILL TURN ON AT END OF CONVERSION.

[2]DRIVERS WILL REMAIN ON IF POWER-DOWN MODE IS 11 (NO POWER DOWN) UNTIL SELECTED INPUT CHANNEL, REFERENCE MODE, OR POWER-DOWN MODE IS CHANGED, OR $\overline{CS}$ IS HIGH.

Figure 14. Conversion Timing, 24 DCLKS per Conversion Cycle, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

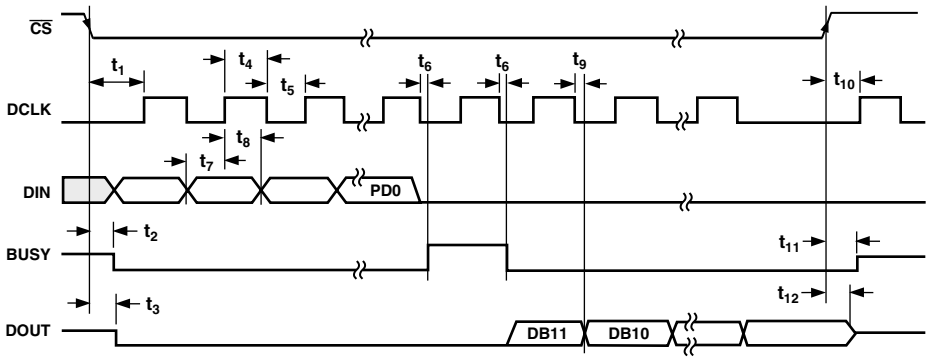


Figure 15. Detailed Timing Diagram

Detailed Serial Interface Timing

Figure 15 shows the detailed timing diagram for serial interfacing to the AD7873. Writing of information to the control register takes place on the first eight rising edges of DCLK in a data transfer. The control register is only written to if a START bit is detected (see Control Register section) on DIN and the initiation of the following conversion is also dependent on the presence of the START bit. Throughout the eight DCLK cycles, when data is being written to the part, the DOUT line will be driven low. The MSB of the conversion result is clocked out on the falling edge of the ninth DCLK cycle and is valid on the rising edge of the tenth DCLK cycle, therefore nine leading zeroes may be clocked out prior to the MSB. This means the data seen on the DOUT line in the 24 DCLK conversion cycle will be presented in the form of nine leading zeroes, twelve bits of data, and three trailing zeroes.

The rising edge of $\overline{CS}$ will put the bus and the BUSY output back into three-state. The DIN line will be ignored, and if a conversion is in progress at the time, then this will also be aborted. However, if $\overline{CS}$ is not brought high after the completion of the conversion cycle, the part will wait for the next START bit to initiate the next conversion. This means each conversion need not necessarily be framed by $\overline{CS}$, as once $\overline{CS}$ goes low the part will detect each START bit and clock in the control word after it on DIN. When the AD7873 is in the 12-bit conversion mode, then a second START bit will not be detected until seven DCLK pulses have elapsed after a control word has been clocked in on DIN, i.e., another START bit can be clocked in on the eighth DCLK rising edge after a control word has been written to the device (see 15 Clock Cycle section). If the device is in the 8-bit conversion mode, a second START bit will not be recognized until three DCLK pulses have elapsed after the control word has been clocked in, i.e., another START bit can be clocked in on the fourth DCLK rising edge after a control word has been written to the device.

Because a START bit can be recognized during a conversion, it means the control word for the next conversion can be clocked in during the current conversion, enabling the AD7873 to complete a conversion cycle in less than 24 DCLKs.

16 Clocks per Cycle

The control bits for the next conversion can be overlapped with the current conversion to allow for a conversion every 16 DCLK cycles, as shown in Figure 16. This timing diagram also allows for the possibility of communication with other serial peripherals between each byte (eight DCLK) transfer between the processor and the converter. However, the conversion must complete within a short enough time frame to avoid capacitive droop effects that may distort the conversion result. It should also be noted that the AD7873 will be fully powered while other serial communications may be taking place between byte transfers.

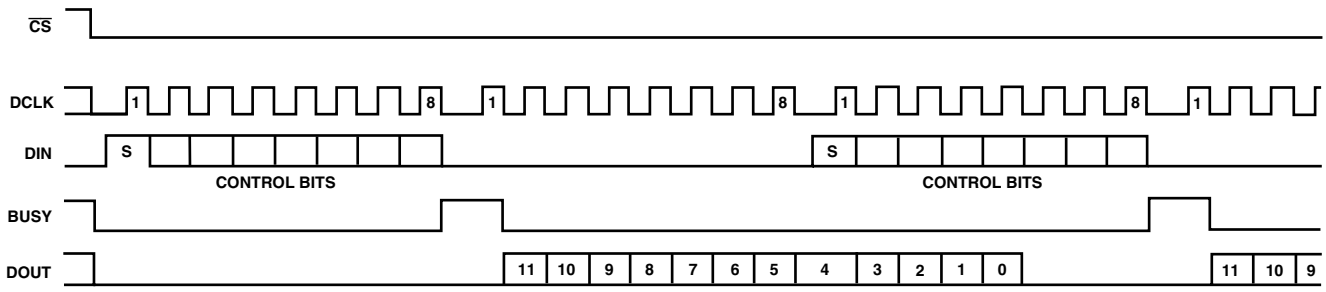


Figure 16. Conversion Timing, 16 DCLKS per Cycle, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

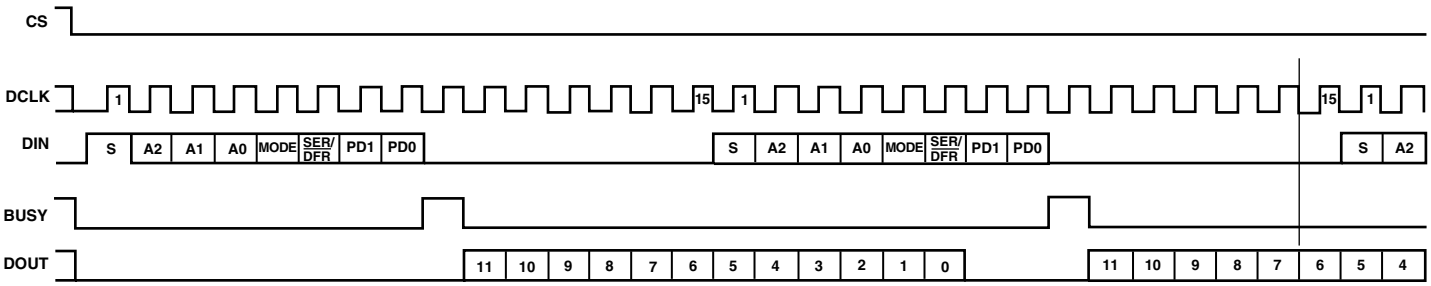


Figure 17. Conversion Timing, 15 DCLKS per Cycle, Maximum Throughput Rate

15 Clocks per Cycle

Figure 17 shows the fastest way to clock the AD7873. This scheme will not work with most microcontrollers or DSPs since they are not capable of generating a 15 clock cycle per serial transfer. However, some DSPs will allow the number of clocks per cycle to be programmed and this method could also be used with FPGAs (field programmable gate arrays) or ASICs (application specific integrated circuits). As in the 16 clocks per cycle case, the control bits for the next conversion are overlapped with the current conversion to allow for a conversion every 15 DCLK cycles using 12 DCLKs to perform the conversion and three DCLKs to acquire the analog input. This will effectively increase the throughput rate of the AD7873 beyond that used for the specifications that are tested using 16 DCLKs per cycle, and DCLK = 2 MHz.

8-Bit Conversion

The AD7873 can be set up to operate in an 8-bit mode rather than 12 bits by setting the MODE bit in the control register to 1. This mode allows a faster throughput rate to be achieved assuming 8-bit resolution is sufficient. When using the 8-bit mode, a conversion is complete four clock cycles earlier than in the 12-bit mode. This could be used with serial interfaces that provide 12 clock transfers, or two conversions could be completed with three eight-clock transfers. The throughput rate will increase by 25% as a result of the shorter conversion cycle, but the conversion itself can occur at a faster clock rate because the internal settling time of the AD7873 is not as critical, as settling to eight bits is all that is required. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide double the conversion rate.

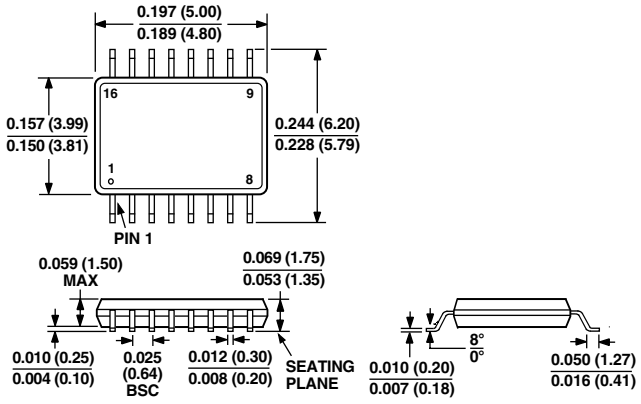
GROUNDING AND LAYOUT

For information on grounding and layout considerations for the AD7873 refer to the "Layout and Grounding Recommendations for Touch Screen Digitizers" Technical Note.

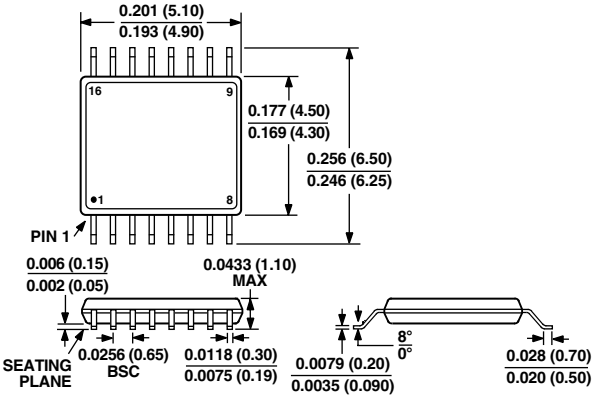
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

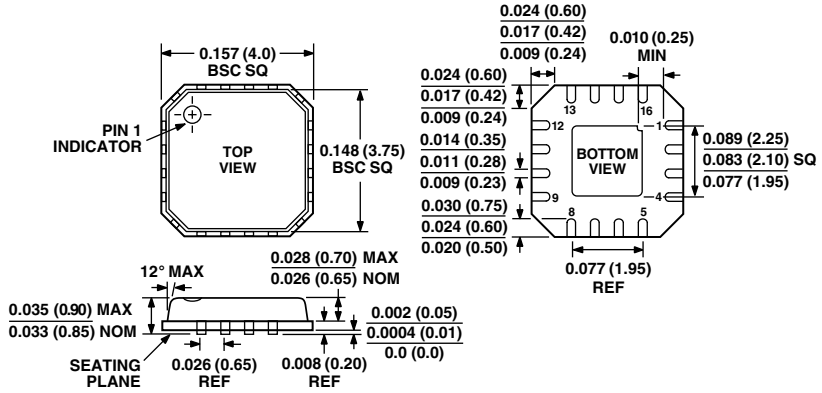
16-Lead QSOP
(RQ-16)



16-Lead TSSOP
(RU-16)



16-Lead LFCSP
(CP-16)



Revision History

Location	Page
01/02—Data Sheet changed from REV. A to REV. B.	
Addition of 16-Lead Lead Frame Chip Scale Package	Universal
Edits to FEATURES	1
Edits to GENERAL DESCRIPTION	1
Addition of LFCSP Pin Configuration	4
Edit to ABSOLUTE MAXIMUM RATINGS	4
Addition to ORDERING GUIDE	4
Addition of CP-16 Outline Dimensions	19
02/01—Data Sheet changed from REV. 0 to REV. A.	
Edits to notes in the ORDERING GUIDE	4

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